REMARKS

Claims 1, 2, 4, 5, and 14-37 are all of the claims pending in the present Application. New claims 28-37 are added. An excess claims fee letter and fee are attached hereto.

Claim 14 is allowed. Applicant gratefully acknowledges the Examiner's indication that claim 27 would be allowable if rewritten in independent format but declines at this time to rewrite this claim in view of the disqualification of Aoki, as explained below. Claims 1, 2, 4, 5 and 15-26 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,096,648 to Lopatin et al., taken in combination with US Patent 6,037,664 to Zhao et al., and US Patent 6,624,061 to Aoki.

However, it is noted that Aoki is disqualified under 35 USC §103(c) as being prior art against the present Application, since it is commonly assigned to NEC Electronics Corporation, and, at the time of the invention, the invention of Aoki and the present invention were commonly owned. Thus, Aoki would qualify only as prior art under §102(e) by reason of the US filing date of May 14, 1999, for Aoki and the Japanese priority date of July 30, 1999, for the present Application. Therefore, Aoki is removed as a prior art reference based on the 35 USC §103(c) "safe harbor".

It is also noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. The Claimed Invention

As described and claimed, for example by claim 1, the present invention is directed to a semiconductor device including a first interlayer insulating layer. A plurality of wiring lines, which are formed of Cu, is formed on the first interlayer insulating layer. An insulating layer which has a property that Cu is unlikely to enter insulates between the plurality of wiring lines. A second interlayer insulating layer is on the insulating layer having a property that Cu is unlikely to enter therein and the plurality of wiring lines.

At least one adhesion layer is formed in an interface between the plurality of wiring lines and the insulating layer. The at least one adhesion layer allows the plurality of wiring lines and the insulating layer to adhere to one another. Each of the at least one adhesion layer

has a polishing rate which is essentially equivalent to a polishing rate of the plurality of wiring lines.

As clearly shown in Figure 10H of the present Application, the TaN barrier conventionally used as the barrier has an etching rate considerably different from that of copper. Therefore, the conventional barrier allows the dishing problem shown in Figure 10H.

II. The Prior Art Rejection

The Examiner alleges that US Patent 6,096,648 to Lopatin et al., in combination with US Patent 6,037,664 to Zhao et al. and US Patent 6,624,061 to Aoki., essentially teaches the invention as described by claims 1, 2, 4, 5, and 15-26. Applicant respectfully disagrees.

It is first noted that the Examiner relies upon Aoki for the rejection of claims 15-26, and the disqualification of Aoki as a prior art reference renders moot the rejection currently of record.

Relative to the rejection for claims 1, 2, 4, and 5, Applicant submits that conventional wisdom, as described beginning at line 22 of page 3 of the specification, for the barrier material for copper lines is TaN. This assertion is confirmed by Zhao, at lines 25-27 of column 5, which indicates that TiN or TaN is preferred with copper as a barrier.

Therefore, it is submitted that similar etching rate between the copper lines and the barrier layer has not been a consideration in the art, previous to the recognition by the present inventor. It is further submitted that recognition of a problem or source of a problem can serve as the basis for patentability, as clearly described at MPEP §2141.02:

"*[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject mater as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. §103.*"

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... a first interlayer insulating layer; a plurality of wiring lines which are formed of Cu, said plurality of wiring lines formed on said first interlayer insulating layer; an insulating layer which has a property that Cu is unlikely to enter said insulating layer and which insulates between said plurality of wiring lines; a second interlayer insulating layer formed on said

insulating layer having a property that Cu is unlikely to enter therein; and at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another, wherein each said at least one adhesion layer has a polishing rate which is essentially equivalent to a polishing rate of said plurality of wiring lines", as required by independent claim 1.

For the reasons stated above, the claimed invention defined by claims 1, 2, 4, and 5 is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Lopatin et al. and/or Zhao et al. fails to teach or suggest the claimed invention

Relative to the new claims, it is disclosed on page 11 at lines 11 to 20 and in Figure 4 that the Cu concentration of the surface region of the insulating layer is equal to 10^{19} atoms/cm^3.

By examining the relationship between the leakage current and the Cu concentration of the insulating layer, the inventor discovered that when the Cu concentration of the insulating layer reaches the order of 10^{19} atoms/cm^3, there is an influence of the leakage current.

In the experiment that the inventor carried out, the Cu concentration in HSQ is in the order of 10^{19} atoms/cm^3 at a position which is 50 nm or less from the contact surface of the HSQ and the Cu wiring lines and is less than 10^{19} atoms/cm^3 at a position which is equal to or more than 50 nm (e.g., see Figure 4).

Therefore, the inventor found that if the thickness of HSQ is equal to or thicker than 50 nm, a device that is not influenced by the leakage current can be obtained. This result was found by the inventor carrying out an experiment, focusing on the relationship between the leakage current and the Cu concentration of the insulating layer. This result is not described or taught in the cited references.

The distribution of Cu concentration of the insulating layer differs by the conditions for forming the insulating layer and the conditions for manufacturing the device. Namely, the distribution of Cu concentration of the insulating layer is not unique to the insulating layer. Therefore, new claims 28 to 37 are not apparent from the cited references.

FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1, 2, 4, 5, and 14-37, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 6/29/04

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